



TRANSMITTAL FORM

Be used for all correspondence after initial filing)

TRANSMITTAL FORM Be used for all correspondence after initial filing)		Application Number	09/916,555
		Filing Date	July 26, 2001
		First Named Inventor	Wang et al.
		Group Art Unit	2814
		Examiner Name	M.D. Pizarro-Crespo
Total Number of Pages in This Submission	15	Attorney Docket Number	2102397-911400

ENCLOSURES (check all that apply)

<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input checked="" type="checkbox"/> Amendment/Reply with Appendix A <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Response to Missing Parts/ Incomplete Application <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Assignment Papers (for an Application) <input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____	<input type="checkbox"/> After Allowance Communication to Group <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below): Return postcard
Remarks		

☒ Customer Number or Bar Code Label

(Insert Customer No. or Attach bar code label here)

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 07-1896. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

GRAY CARY WARE & FREIDENRICH LLP

Dated: October 22, 2002

By:

Alan A. Limbach
 Reg. No. 39,749
 Attorneys for Applicant(s)

Gray Cary Ware & Freidenrich LLP
 1755 Embarcadero Road, Palo Alto, CA 94303-3340

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, DC 20231 on this date: October 22, 2002

Typed or printed name	Kathleen LaBrie	Date	October 22, 2002
Signature	<u>Kathleen LaBrie</u>		



Atty Dekt Number: 2102397-911400

PATENT

- 1 -

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Chi Hsin Wang et al.

Application No. 09/916,555

Filed: July 26, 2001

For: A SEMICONDUCTOR MEMORY
ARRAY OF FLOATING GATE
MEMORY CELLS WITH LOW
RESISTANCE SOURCE REGIONS AND
HIGH SOURCE COUPLING
(as amended herein)

Group Art Unit: 2814

Examiner: M. D. Pizarro-Crespo

**RESPONSE TO OFFICE ACTION
MAILED JULY 26, 2002**

1755 Embarcadero Road
Palo Alto, CA 94303-3340
(650) 833-2000

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Box, Assistant Commissioner for Patents, Washington, DC 20231, on October 22, 2002.

GRAY CARY WARE & FREIDENRICH Date: 10/22/02

By: *Kathleen LaBrie*

Kathleen LaBrie

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed on July 26, 2002 please amend the above identified application as follows:

I. CLEAN VERSION OF AMENDED SPECIFICATION, TITLE AND CLAIMS,
AND NEWLY ADDED CLAIMS

✓ A. Please amend the title to read:

--A SEMICONDUCTOR MEMORY ARRAY OF FLOATING GATE MEMORY
CELLS WITH LOW RESISTANCE SOURCE REGIONS AND HIGH SOURCE COUPLING--

B. Please substitute the paragraph on page 12, lines 4-24 with the following paragraph:

--As shown in Fig. 2N, first and second regions 50/80 form the source and drain for each cell (those skilled in the art know that source and drain can be switched during operation). The channel region 92 for each cell is the portion of the substrate that is in-between the source and drain 50/80. Poly blocks 68 constitute the control gate, and poly layer 14 constitutes the floating gate. Oxide layers 32, 36, 46 and 48 together form an insulation layer that is disposed adjacent to and over floating gate 14, to isolate it from conductive block 54 and conductive layer 52. Oxide layers 36 and 64 together form an insulation layer that isolates the conductive block 54 and conductive layer 52 from the control gates 68. The control gates 68 have one side aligned to the edge of the second region 80, and are disposed over part of the channel regions 92. Control gates 68 have lower portions 70 that are disposed adjacent to the floating gates 14 (insulated therefrom by oxide layer 64), and upper protruding portions 72 that are disposed (extend) over a portion of adjacent poly layers 14 (insulated therefrom by oxide layers 64). A notch 94 is formed by the protruding portion 72, where the sharp edge 66 of floating gate 14 extends into the notch 94. Each floating gate 14 is disposed over part of the channel region 92, is partially overlapped at one end by the control gate 68, and partially overlaps the first region 50 with its other end. Conductive blocks 54 and the conductive layers 52/56 together form source lines 96 that extend across the columns of memory cells. Upper portions 62 of source lines 96 extend over but are insulated from the floating gates 14, while lower portions 60 of source lines 96 are adjacent to but insulated from floating gates 14. As illustrated in the Fig. 2N, the process of the present invention forms pairs of memory cells that mirror each other. The pairs of mirrored memory cells are insulated from other cell pairs by oxide layer 76, nitride spacers 78 and BPSG 86.--

C. Please substitute each of the following claims for the corresponding pending claim in this application:

27. (Amended) An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart regions of a second conductivity type formed in the substrate, with a channel region therebetween;

an electrically conductive floating gate disposed over and insulated from a portion of said channel region and a portion of the first region, wherein the floating gate consists of a first portion and a second portion integrally formed together;

an electrically conductive source region disposed over and electrically connected to the first region in the substrate, the source region having a lower portion that is disposed adjacent to and insulated from the floating gate and an upper portion that is disposed over and insulated from the floating gate first portion and not the floating gate second portion; and

an electrically conductive control gate having a first portion and a second portion, the first control gate portion being disposed adjacent to and insulated from the floating gate, and the second control gate portion being disposed over and insulated from the floating gate second portion and not the floating gate first portion.

30. (Amended) The device of claim 27, further comprising:

an insulation layer disposed between the floating gate and the control gate, and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

31. (Amended) An array of electrically programmable and erasable memory devices comprising:

a substrate of semiconductor material of a first conductivity type;

spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions; and

each of the active regions including a column of pairs of memory cells extending in the first direction, each of the memory cell pairs including:

sub
act.
a first region and a pair of second regions spaced apart in the substrate and having a second conductivity type, with channel regions formed in the substrate between the first region and the second regions,

12
13
14
a pair of electrically conductive floating gates each disposed over and insulated from a portion of one of the channel regions and a portion of the first region, wherein each of the floating gates consists of a first portion and a second portion integrally formed together,

15
16
17
an electrically conductive source region disposed over and electrically connected to the first region in the substrate, the source region having a lower portion that is disposed adjacent to and insulated from the pair of floating gates and an upper portion that is disposed over and insulated from the floating gate first portions and not the floating gate second portions; and

a pair of electrically conductive control gates each having a first portion and a second portion, wherein for each of the control gates, the first control gate portion is disposed adjacent to and insulated from one of the floating gates and the second control gate portion is disposed over and insulated from the second portion and not the first portion of the one floating gate.

18
19
20
35. (Amended) The device of claim 31, wherein each of the memory cell pairs further comprises:

an insulation layer disposed between each of the floating gates and each of the control gates and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

D. Please add the following new claims:

37. (New) The device of claim 27, further comprising:
insulation material disposed between the source region second portion and the floating gate first portion, and having a thickness for permitting voltage coupling therebetween.

38. (New) The device of claim 31, wherein each of the memory cell pairs further comprises:
insulation material disposed between the source region second portion and each of the floating gate first portions, and having a thickness for permitting voltage coupling therebetween.